IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Seiji SHIRAI et al.

Serial No : 09/600,890 Group Art Unit: 2827

Filed : August 16, 2000 Examiner: Tuan DINH

For : MULTILAYER PRINTED WIRING BOARD WITH FILLED VIAHOLE STRUCTURE

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450`

Sir:

This Appeal is from the Examiner's Final Rejection of claims 1-3, 5-12, 14-19, and 21-36 as set forth in the Final Office Action mailed on November 19, 2003 and modified by the Advisory Action of February 13, 2004. A Notice of Appeal in response to the Final Rejection was filed on April 19, 2004. The requisite fee under 37 C.F.R.§1.17(C) in the amount of $330.00 is being paid by check, submitted herewith. Appellants are concurrently filing an amendment with this Appeal Brief in order to reduce issues on appeal.

Inasmuch as the two-month period for filing the Appeal Brief ends on June 19, 2004, this Appeal Brief is being filed in a timely manner and no extension of time is required. However, the Commissioner is hereby authorized to charge any necessary fees, such as any necessary extension of time fees to Deposit Account No. 19-0089.

This Appeal Brief is being submitted in triplicate.

I. REAL PARTY IN INTEREST

The real party in interest is IBIDEN Co., Ltd., Japan, by an assignment which was recorded on August 16, 2000, at Reel/Frame 011045/0540.

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any other appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3, 5-12, 14-19, and 21-36 are currently pending in this application. Claims 1, 9, 17, and 25 are independent claims. The Advisory Action of record indicates that claims 1-3, 5-12, 14-19, and 21-36 remain rejected, for purposes of appeal.

The claims under appeal, i.e., claims 1-3, 5-12, 14-19, and 21-36, are reproduced in the Appendix attached hereto. Cancellation of claim 11 is requested via a concurrently filed Amendment.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Rejection, a Response Under 37 C.F.R. §1.116 was filed on January 20, 2004. However, the Advisory Action indicated that the Response of January 20, 2004 is not deemed to place the application in condition for allowance.

V. SUMMARY OF INVENTION

A multilayer printed wiring board has many layers of wiring board that are electrically connected to each other by viaholes formed in insulative resin layers. Generally, the viaholes in such a multilayer printed wiring board are formed by depositing a plating metal film on the inner wall and bottom of each of fine holes formed through the interlaminar insulative resin layers. However, the multilayer printed wiring board having such viaholes presents problems in that the metal deposit is likely to break due to precipitation or stress resulting from heat cycles. To avoid this problem, it has recently been proposed to fill the viaholes with a plating metal.

The multilayer printed wiring board having the filled viahole structure is however disadvantageous in that a surface portion of the plating metal exposed outside the hole is easily depressible. If an interlaminar insulating layer resin is formed on a conductor circuitry layer, a corresponding depression will develop on the surface of the interlaminar insulative resin layer, and cause the plating metal film to break. The viahole surface where such a depression exists can be flattened by applying interlaminar resin layers more than once. However, the additional application of the interlaminar resin will lead to a greater thickness of the interlaminar insulative resin layer above the depression on the viahole surface.

The present invention addresses these problems by providing a multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having a substantially flat surface to form a viahole having a diameter; wherein the surface of said plating layer extends out of the through-holes and lies in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies; at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm; and the thickness of the conductor circuit layer is less than a half of the viahole diameter.

The present invention also provides a multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having at least one surface to form a viahole having a diameter, wherein depressions are formed on a central surface portion of the plating layer surface extending out of the through-holes, and wherein the thickness of said conductor circuit layer is less than a half of the viahole diameter and less than 25 μm and wherein at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm.

The present invention also provides a multilayer printed wiring board comprising conductor circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer is roughened to a depth of 1 to 10 μm and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall wherein the inner wall is roughened, substantially filled up with a plating layer to form a viahole, wherein the roughened inner wall is covered with a roughened electroless plating layer; and an inner space of the through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.

The present invention also provides a multilayer printed wiring board comprising conductor circuit layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall, substantially filled up with a plating layer to form a viahole, said interlaminar insulative resin layers being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

In this regard, Appellant notes that these embodiments are reflected in independent claims 1, 9, 17, and 25 respectively.

Turning now to the dependent claims, Appellant notes that the dependent claims claim additional features of preferred embodiments of the present invention.

VI. ISSUES

A. Whether claim 11 is properly rejected under 35 U.S.C.§112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

Claim 11 is rejected under 35 U.S.C.§112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. Specifically, the Examiner states that the claim recitation of claim 11, lines 2-3 is confusing.

B. Whether claims 1-2, 6-11, 15-18, 22-25, 27-28, 30, and 32-36 are properly rejected under 35 U.S.C.§102(e) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO")

Thus, the issue under consideration is whether UNO discloses all of the elements of these rejected claims.

C. Whether claims 3, 12, 19, 29 are properly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 5,509,200 ("FRANKENY")

The Final Office Action indicates that UNO discloses all of the elements of the rejected claims except for the plating layer surface being roughened. The Final Office Action relies on FRANKENY as a secondary document and states that FRANKENY shows a plating layer having a roughened surface. The Final Office Action concludes that it would

have been obvious to have a roughened surface on a plating layer in UNO to provide a reliable electrical connection, seal a boundary, and bind two or more stackable layers into the multi-layer circuit board. Thus an issue under consideration is whether the combination of UNO and FRANKENY establishes a prima facie case of obviousness.

D. Whether claims 5, 14, 21, 31 are properly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 6,127,633 ("KINOSHITA")

The Final Office Action alleges that UNO discloses all of the elements of these claims except for the recitation of a further viahole being formed in the viahole. The Final Office Action further states that KINOSHITA shows a structure of wiring board having a further viahole formed in a viahole. Thus an issue under consideration is whether the combination of UNO and KINOSHITA establishes a prima facie case of obviousness.

E. Whether claim 26 is properly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 4,769,270 ("NAGAMATSU")

The Final Office Action alleges that NAGAMATSU shows an insulating layer made of a composite of fluororesin fiber cloth, wherein the cloth comprises voids and the thermosetting resin is impregnated in the voids in the cloth. The Final Office Action concludes that it would have been obvious to employ NAGAMATSU's material in UNO in order to "achieve high performance in ["if"] a high region has been desired." Thus an issue under consideration is whether the combination of UNO and NAGAMATSU establishes a

prima facie case of obviousness.

VII. GROUPING OF CLAIMS

For each ground of rejection included in the Examiner's Final Rejection which applies to more than one claims, the rejected claims do not stand or fall together for the following reasons. For example, while the Examiner has rejected claims 1, 2, and 6 under 35 U.S.C. §102(e), claims 2 and 6 depend from claim 1 but are separately patentable because claim 2 claims a preferred board wherein the inner wall of the through-hole is roughened and claim 6 claims a preferred board wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

VIII. ARGUMENTS

The Examiner's November 19, 2003 Final Office Action and February 13, 2004 Advisory Action are the subject of this appeal.

A. Claim 11 is improperly rejected under 35 U.S.C.§112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

From the Advisory Action, it appears that the Examiner rejected claim 11 under 35 U.S.C. §112, fourth paragraph, not second paragraph. Upon further consideration, Appellant is currently filing an amendment to cancle claim 11.

B. Claims 1-2, 6-11, 15-18, 22-25, 27-28, 30, and 32-36 are improperly rejected under 35 U.S.C.§102(e) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO").

"A prior art reference anticipates a patent claim if the reference discloses, either expressly or inherently, all of the limitations of the claim." EMI Group N. Am., Inc., v. Cypress Semiconductor Corp., 268 F3d 1342, 1350 (Fed. Cir. 2001).

UNO does not disclose all of the recitations of the rejected claims and the rejection is improper and should be reversed on this basis alone.

Specifically, Appellants respectfully submit that UNO fails to teach or suggest "through-holes having an inner wall substantially filled up with a plating layer having a substantially flat surface...." as recited in independent claims 1, 9, 17, and 25. The recitation of "filled up" in these claims indicates that the inner wall is substantially and completely filled with a plating layer. For example, as disclosed in Figure 2b of the present application, the through-holes (10) in the interlaminar insulative resin layer are substantially and completely filled with electroplating layer (9). UNO also fails to teach or suggest the recitation of claim 9 "wherein depressions are formed on a central surface portion of the plating layer surface extending out of the through-holes, ..." The present invention is directed to an arrangement of filled through holes, *i.e.*, through holes filled completely or substantially completely with electric conductive materials, adapted to form a fine conductor circuit pattern and provide highly reliable electrical connection between

the conductive circuit layers, thus assuring a highly secure adhesion between the conductive circuit layer and interlaminar insulative resin layer. In contradistinction, the through holes of UNO are formed by the plating layer being deposited on the inner wall of the through-hole, not formed by the plating layer filled completely in the through-hole. In view of this difference alone, among others, the rejection should be reversed.

Referring to figure 5 of UNO, the Final Office Action states that UNO discloses a through hole (7) having an inner wall substantially filled up with a plating layer. Appellants respectfully submit that the through hole in Figure 5 is the reference number 8, not 7 as clearly described in lines 9-10, col 13 of the specification of UNO. Clearly, as can be seen in Figure 5, the through holes of UNO are not substantially filled up with any plating layers. Therefore, the Examiner's interpretation of UNO is mistaken and the rejection based on UNO should be reversed.

Additionally, each of the dependent claims which are also the subject of this rejection is patentable over the cited document at least because each of these dependent claims includes additional recitations. For example, for rejected dependent claims that depend from claim 1, claim 2 recites a multilayer printed wiring board "wherein the inner wall of the through-hole is roughened;" claim 6 recites a multilayer printed wiring board "wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins;" claim

7 recites a multilayer printed wiring board "wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4;" claim 8 recites a multilayer printed wiring board "wherein the conductor circuit layer has a thickness less than 25 μm." These additional recitations along with all recitations of the independent claims are not all disclosed in UNO.

In view of the above, Appellant respectfully requests that the rejection of these claims be reversed.

C. Claims 3, 12, 19, 29 are improperly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 5,509,200 ("FRANKENY").

Appellants respectfully submit that the combination of UNO and FRANKENY, even assuming, arguendo, that a proper suggestion or motivation for the combination exists, still fails to disclose or suggest that the through-hole be "substantially filled up with a plating layer." For this reason alone, the obviousness rejections should be reversed.

Further, there must be some suggestion or motivation to combine the documents for such combination to be proper. There must be a teaching or suggestion within the prior art, or within the general knowledge of a person of ordinary skill in the field of the invention, to look to particular sources of information, to select particular elements, and to combine them in the way they were combined by the inventor. ATD Corporation v. Lydall, Inc., 48 USPQ2d 1321, 1329 (Fed. Cir. 1998). In other words, "defining the problem in terms of

its solution reveals improper hindsight in the selection of the prior art relevant to obviousness." Monarch Knitting Machinery Corp. et al. v. Sulzer Morat Gmbh, et al., 45 USPQ2d 1977, 1981 (Fed. Cir. 1998) (citing In re Antle, 444 F.2d 1168, 1171-72, 170 USPQ 285, 287-88 (CCPA 1971)).

In the present case, the alleged suggestion or motivation of providing "a reliable electrical connection, seal a boundary, and bind two or more stackable layers into the multi-layer circuit board" is not suggested or disclosed in either document but is a mere allegation in the Final Office Action. Moreover, this "allegation" is not substantiated anywhere in the Final Office Action by any evidence advanced by the Examiner. Therefore, the Final Office Action has not established a *prima facie* case of obviousness and the rejections should be reversed.

D. Claims 5, 14, 21, 31 are improperly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 6,127,633 ("KINOSHITA").

Appellants respectfully submit that the combination of UNO and KINOSHITA, even assuming, arguendo, that a proper suggestion or motivation for such a combination exists, still fails to disclose or suggest that the through-hole be "substantially filled up with a plating layer." For this reason alone, the obviousness rejection of these claims should be withdrawn.

Further and again, the alleged suggestion or motivation of providing "an electrical

contact of each layer of a multiplayer wiring board" is not suggested or disclosed in either document, but is a mere allegation in the Final Office Action. Moreover, this "allegation" is not substantiated anywhere in the Final Office Action by any evidence advanced by the Examiner. Therefore, the Final Office Action has not established a *prima facie* case of obviousness and the rejection should be reversed.

E. Claim 26 is improperly rejected under 35 U.S.C.§103(a) as being unpatentable over U.S. Patent No. 5,827,604 ("UNO") in view of U.S. Patent No. 4,769,270 ("NAGAMATSU").

Appellants respectfully submit that the combination of UNO and NAGAMATSU, even assuming, arguendo, that a proper suggestion or motivation exists for the combination, still fails to disclose or suggest that the through-hole is "substantially filled up with a plating layer." For this reason alone, the obviousness rejection of this claim should be reversed.

Appellants further submit that contrary to the recited composite of fluororesin fiber cloth and thermoplastic resin, NAGAMATSU's inorganic fiber cloth (layer 4) is distinct (therefore not a composite of the two) from the thermoplastic resin layer 3. Therefore, NAGAMATSU does not disclose or suggest a composite as recited in claim 26. Also for this reason alone, this rejection should be reversed.

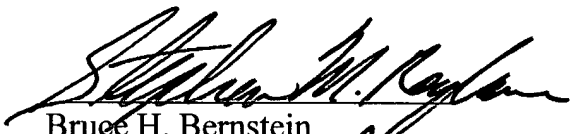
Further, the alleged suggestion or motivation of achieving "high performance in a high region has been desired" is not suggested or disclosed in either document, but is a mere

unsubstantiated allegation by the Examiner. Therefore, the Final Office Action has not established a *prima facie* case of obviousness and the rejection should be reversed.

IX. CONCLUSION

For the reasons set forth above, it is respectfully submitted that the Examiner has improperly rejected all pending claims. The Board is, therefore, respectfully requested to reverse the Final Rejection, and to allow the application to issue.

Respectfully submitted,
Seiji SHIRAI et al.



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Appendix

CLAIMS:

1. A multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having a substantially flat surface to form a viahole having a diameter; wherein:

the surface of said plating layer extends out of the through-holes and lies in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies;

at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm; and

the thickness of said conductor circuit layer is less than a half of the viahole diameter.

2. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the through-hole is roughened.

3. The multilayer printed wiring board as set forth in Claim 1, wherein the plating layer surface and conductor circuit layer extending out of the through-holes are roughened.

5. The multilayer printed wiring board as set forth in Claim 1, wherein a further viahole is formed in the viahole.

6. The multilayer printed wiring board as set forth in claim 1, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

7. The multilayer printed wiring board as set forth in Claim 1, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

8. The multilayer printed wiring board as set forth in Claim 1 , wherein the conductor circuit layer has a thickness less than 25 μm.

9. The multilayer printed wiring board comprising conductor circuit layers each having a respective thickness and a surface and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes having an inner wall substantially filled up with a plating layer having at least one surface to form a viahole having a diameter, wherein depressions are formed on a central surface portion of the plating layer surface extending out of the through-holes, and wherein the thickness of said conductor circuit layer is less than a half of the viahole diameter and less than 25 μm and wherein at least one of the surfaces of the conductor circuits is roughened to a depth of 1 to 10 μm.

10. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the through-holes is roughened.

11. The multilayer printed wiring board as set forth in Claim 9, wherein a depression is formed on a central surface portion of the plating layer surface extending out of the through-hole.

12. The multilayer printed wiring board as set forth in Claim 9 , wherein the surface of the plating layer and the surface of the conductor circuit layer extending out of the through-holes are roughened.

14. The multilayer printed wiring board as set forth in Claim 9 , wherein a further viahole is formed in the viahole.

15. The multilayer printed wiring board as set forth Claim 9, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

16. The multilayer printed wiring board as set forth in Claim 9, wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

17. A multilayer printed wiring board comprising conductor circuit layers each with at least one surface wherein at least one of the surfaces of the conductor circuit layer is roughened to a depth of 1 to 10 μm and interlaminar insulative resin layers deposited

alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall wherein the inner wall is roughened, substantially filled up with a plating layer to form a viahole, wherein:

said roughened inner wall is covered with a roughened electroless plating layer; and

an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.

18. The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes .

19. The multilayer printed wiring board as set forth in Claim 17 , wherein the plating layer surface and conductor circuit surface extending out of the through-holes are roughened.

21. The multilayer printed wiring board as set forth in Claim 17, wherein a further viahole is formed in the viahole.

22. The multilayer printed wiring board as set forth in any of Claims 17, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

23. The multilayer printed wiring board as set forth in Claim 17 , wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a

range of 1 to 4.

24. The multilayer printed wiring board as set forth in Claim 17 , wherein the conductor circuit layer has a thickness less than 25 μm.

25. A multilayer printed wiring board comprising conductor circuit layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having through-holes, having an inner wall, substantially filled up with a plating layer to form a viahole, said interlaminar insulative resin layers being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth, wherein said cloth comprises voids, and wherein a composite of thermosetting resin is impregnated in the voids in the cloth.

27. The multilayer printed wiring board as set forth in Claim 25, wherein the inner wall of the through-hole is roughened.

28. The multilayer printed wiring board as set forth in Claim 25, wherein depressions are formed in the central surface portion of the plating layer surface extending out of the through-holes.

29. The multilayer printed wiring board as set forth in Claim 25 , wherein the plating layer surface and conductor circuit surface extending out of the hole for the through-holes are roughened.

30. The multilayer printed wiring board as set forth Claim 25, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

31. The multilayer printed wiring board as set forth in Claim 25 , wherein a further viahole is formed in the viahole.

32. The multilayer printed wiring board as set forth in Claim 25 , wherein a ratio between the viahole diameter and interlaminar insulative resin layer thickness is within a range of 1 to 4.

33. The multilayer printed wiring board as set forth in Claim 25, wherein the conductor circuit layer has a thickness less than 25 μm.

34. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened electroless plating layer, and an inner space of said through-holes defined by the electroless plating layer is filled up with an electroplating layer.

35. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened electroless

plating layer, and an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.

36. The multilayer printed wiring board as set forth in Claim 25, wherein the inner wall is roughened, and the roughened inner wall is covered with a roughened electroless plating layer, and an inner space of said through-holes defined by the electroless plating layer is substantially filled up with an electroplating layer.